Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (previously presented) An integrated circuit comprising:

a plurality of memory cells coupled in series to form a series group, the memory cells of a group are arranged in memory cell pairs, a memory cell pair of the group comprises;

a first memory cell having a first transistor having a gate and first and second diffusion regions and a first capacitor having first and second plates separated by a first capacitor dielectric;

a second memory cell having a second transistor having a gate and first and second diffusion regions and a second capacitor having first and second plates separated by second capacitor dielectric;

the second diffusion regions of the first and second transistors of the memory cell pair is a common second diffusion region;

the first and second capacitors are arranged in a stack in which the second plates of the capacitors is a common second plate;

the first plate of the first capacitor is coupled to the first diffusion region of the first transistor;

the first plate of the second capacitor is coupled to the first diffusion region of the second transistor; and

the common second plate is coupled to the common second diffusion region.

2. (previously presented) The integrated circuit of claim 1 wherein the memory cells are ferroelectric memory cells in which the capacitor dielectrics comprise a ferroelectric material.

3. (previously presented) The integrated circuit of claim 2 wherein the first plate of the first capacitor is coupled to the first diffusion region of the first transistor via a bottom first plate plug.

4. (previously presented) The integrated circuit of claim 2 wherein the common second plate is coupled to the common second diffusion via an active common second plate plug which is isolated from the first capacitor dielectric and first plate of the first capacitor.

5. (previously presented) The integrated circuit of claim 4 wherein the first plate of the first capacitor is coupled to the first diffusion region of the first transistor via a bottom first plate plug.

6. (previously presented) The integrated circuit of claim 1 wherein the first plate of the first capacitor is coupled to the first diffusion region of the first transistor via a bottom first plate plug.

7. (previously presented) The integrated circuit of claim 1 wherein the common second plate is coupled to the common second diffusion via an active common second plate plug which is isolated from the first capacitor dielectric and first plate of the first capacitor.

8. (previously presented) The integrated circuit of claim 6 wherein the first plate of the first capacitor is coupled to the first diffusion region of the first transistor via a bottom first plate plug.

9. (currently amended) The integrated circuit of any one of claims 1-8 wherein first diffusion region of the second transistor of a first memory cell pair of adjacent memory cell pairs and the first diffusion region of the first transistor of a second memory cell pair of the adjacent memory cell pairs is a common first diffusion region of the adjacent memory cell pairs.

10. (previously presented) The integrated circuit of claim 9 wherein the first electrode of the second capacitor of the first adjacent memory cell pair is coupled to the first electrode of the first electrode of the first capacitor of the second adjacent memory cell pair and the common first diffusion region of the adjacent memory cell pairs.

11. (new) A method for forming an integrated circuit comprising:

providing a substrate prepared with at least a partially formed memory cell pair of a series group, the partially formed memory cell pair comprises first and second transistors having first diffusion regions and a common second diffusion region, a dielectric layer on the substrate covering the first and second transistors, bottom electrode plugs formed in the dielectric layer coupling to the first diffusion regions and a lower portion of a common electrode plug formed in the dielectric layer coupling to the common diffusion region;

forming first subcapacitors of first and second capacitors, the first subcapacitors comprising a bottom electrode, a first capacitor dielectric layer above the bottom electrode, and a common electrode above the first capacitor dielectric layer, wherein the bottom electrode extends beyond the first capacitor dielectric layer and common electrode, the bottom electrode of the first subcapacitor of the first capacitor is coupled to the bottom electrode plug coupled to the first diffusion region of the first transistor and the bottom electrode of the first subcapacitor of the second capacitor is coupled to the bottom electrode plug coupled to the first diffusion region of the second transistor;

forming a first intermediate dielectric layer over the substrate, the surface of the first intermediate dielectric layer being substantially coplanar with top surfaces of the first subcapacitors;

forming an upper portion of the common electrode plug in the intermediate dielectric layer, coupling the common plate of the first subcapacitor of the first capacitor with the common diffusion region, the upper portion of the common electrode plug being isolated from the bottom electrode and capacitor dielectric of the first subcapacitors;

forming second subcapacitors above first subcapacitors, the second subcapacitors each having a common electrode with the first capacitors, a second capacitor dielectric layer and a top electrode; and

forming a series plug for coupling the top electrode of the first capacitor to the bottom electrode of the second capacitor.

12. (new) The method of claim 11 further comprises:

forming a top electrode plug coupling to the top electrode of the second subcapacitor of the first capacitor; and

forming a conductive strip coupling the top electrode plug to the series plug.

13. (new) The method of claim 11 wherein the capacitor dielectric layers comprise a ferroelectric material.

14. (new) The method of claim 13 further comprises:

forming a top electrode plug coupling to the top electrode of the second subcapacitor of the first capacitor; and

forming a conductive strip coupling the top electrode plug to the series plug.